ABSTRACT

TOP GATE THIN-FILM TRANSISTOR AND METHOD OF PRODUCING THE SAME

A method of producing a top gate thin-film transistor comprises the steps of forming doped silicon source and drain regions (6a,8a) on an insulating substrate (2) and subjecting the face of the substrate (2) on which the source and drain regions (6a,8a) are formed to plasma treatment to form a doped surface layer. An amorphous silicon layer (12) is formed on the doped surface layer over at least the spacing between the source and drain regions (6a,8a) and an insulated gate structure (14,16) is formed over the amorphous silicon layer (12). Laser annealing of areas of the amorphous silicon layer not shielded by the gate conductor is carried out to form polysilicon portions (12a,12b) having the impurities diffused therein. In the method of the invention, doped silicon source and drain regions underlie the silicon layer to be crystallized using the laser annealing process. It has been found that the laser annealing process can then result in crystallization of the full thickness of the amorphous silicon layer. This results from the similar thermal properties of the doped source and drain regions and the silicon layer defining the main body of the transistor.